ABSTRACT

An IC solution utilizing mixed FPGA and MLC arrays is proposed. The process technology is based on the Schottky CMOS devices comprising of CMOS transistors, low barrier Schottky barrier diode (SBD), and multi-level cell (MLC) flash transistors. Circuit architectures are based on the pulsed Schottky CMOS Logic (SCL) gate arrays, wherein a variable threshold NMOS transistor may replace the regular switching transistor. During initialization windows, existing FPGA programming techniques can selectively adjust the VT of the switching transistor, re-configure the intra-connections of the simple SCL gates, complete all global interconnections of various units. Embedded hardware arrays, hardwired blocks, soft macro constructs in one chip, and protocols implementations are parsed. A wide range of circuit applications involving generic IO and logic function generation, ESD and latch up protections, and hot well biasing schemes are presented.

The variable threshold transistors thus serve 3 distinctive functions. It acts as an analog device to store directly nonvolatile information in SCL gates. It couples the diode tree logic functions. Finally, it stores and operates large amount of information efficiently. The mixed SCL type FPGA and MLC storages shall emerge as the most compact logic and memory arrays in Si technology. Low power, high performance, and high capacity ICs are designed to mix and replace conventional CMOS-TTL circuits. The idea of multi-value logic composed of binary, ternary, and quaternary hardware and firmware is also introduced.